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WHAT IS CLAIMED IS:

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1. An apparatus for processing data, said apparatus comprising:

a special register bank of N-bit data processing registers;

a general register bank of N-bit data processing registers;

a selector, coupled to the special register bank and the general register bank, for selecting one of the special and general register banks and outputting a selected N-bit result from the selected register bank, wherein the selected N-bit result and a N-bit data form a 2N-bit addition operand;

a multiplier for performing multiply operation upon a first operand and a second operand and outputting an 2N-bit multiplied result;

an accumulator, coupled to the multiplier, the selector and the general register bank, for performing accumulate operation upon the 2N-bit multiplied result and the 2N-bit addition operand and outputting a 2N-bit accumulated result.

2. The apparatus for processing data of claim 1, wherein the N-bit data is held in the general register bank.

3. The apparatus for processing data of claim 1, the selector further receiving a class signal, wherein the selector selects one of the special and general register banks in response to the class signal.

4. The apparatus for processing data of claim 3, the class signal is used for indicating a first class of instruction or a second class of instruction, wherein the first class of instruction is executing a first calculation of $N*N+2N \rightarrow 2N$ and the second class of instruction is executing a second calculation of $N*N+N \rightarrow N$.

Cont A1

5. The apparatus for processing data of claim 4, the apparatus further comprising a detecting device, coupled to the accumulator, for receiving the 2N-bit accumulated result and for checking if a case of overflow occurs.

6. The apparatus for processing data of claim 5, wherein

the outputted N-bit result from the selector and the N-bit data held in the general register bank are formed in combination as a first N-bit part and a second N-bit part of the 2N-bit addition operand,

the accumulated result includes a third N-bit part and a forth N-bit part,

when the class signal is the second class of instruction, the detecting device comparing the first N-bit part of the 2N-bit addition operand and the third N-bit part of the accumulated result to determine if the case of overflow occurs.

7. The apparatus for processing data of claim 1, the apparatus further comprising a detecting device, coupled to the accumulator, for receiving the 2N-bit accumulated result and for checking if a case of overflow occurs.

8. The apparatus for processing data of claim 7, wherein

the outputted N-bit result from the selector and the N-bit data are formed in combination as a first N-bit part and a second N-bit part of the 2N-bit addition operand,

the accumulated result includes a third N-bit part and a forth N-bit part,

when the class signal is the second class of instruction, the detecting device comparing the first N-bit part of the 2N-bit addition operand and the third N-bit part of the accumulated result to determine if the case of overflow occurs.

9. A method for processing data using an apparatus having a special register bank of N-bit data processing registers, a general register bank of N-bit data processing registers, a selector, a multiplier and an accumulator, the method comprising:

A1

selecting one of the special and general register banks and outputting a N-bit result from the selected register bank, wherein the N-bit result and a N-bit data form a 2N-bit addition operand;

performing multiply operation upon a first operand and a second operand and outputting an 2N-bit multiplied result;

performing accumulate operation upon the 2N-bit multiplied result and the 2N-bit addition operand and outputting a 2N-bit accumulated result.

10. The method for processing data of claim 9, wherein the N-bit data is held in the general register bank.

11. The method for processing data of claim 10, wherein the step of selecting one of the special and general register banks and outputting N-bit data from the selected register banks further comprising a step of receiving a class signal is determined by a class signal received by the selector.

12. The method for processing data of claim 11, the class signal is used for indicating a first class of instruction or a second class of instruction, wherein the first class of instruction is executing a first calculation of $N*N+2N \rightarrow 2N$ and the second class of instruction is executing a second calculation of $N*N+N \rightarrow N$.

13. The method for processing data of claim 12, further comprising a step of receiving the 2N-bit accumulated result and checking if a case of overflow occurs.

14. The method for processing data of claim 13, wherein

the outputted N-bit result from the selector and the N-bit data held in the general register bank are formed in combination as a first N-bit part and a second N-bit part of the 2N-bit addition operand,

the accumulated result includes a third N-bit part and a forth N-bit part,

A1

when the class signal is the second class of instruction, comparing the first N-bit part of the 2N-bit addition operand and the third N-bit part of the accumulated result to determine if the case of overflow occurs.

15. The method for processing data of claim 9, further comprising a step of receiving the 2N-bit accumulated result and checking if a case of overflow occurs.

16. The method for processing data of claim 15, wherein

the outputted N-bit result from the selector and the N-bit data are formed in combination as a first N-bit part and a second N-bit part of the 2N-bit addition operand,

the accumulated result includes a third N-bit part and a forth N-bit part,

when the class signal is the second class of instruction, comparing the first N-bit part of the 2N-bit addition operand and the third N-bit part of the accumulated result to determine if the case of overflow occurs.